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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,338	12/31/2003	Peter N. Martin	42P17996	4703

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Jan Little-Washington
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
MISIURA, BRIAN THOMAS	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,338	MARTIN ET AL.	
	Examiner	Art Unit	
	Brian T. Misiura	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claim 8-10, 16-18, 22, 25-26, 28-29 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. "approximately fifty percent" is not clear and concise.

Claim Rejections - 35 USC § 101

2. Claims 17-24 are directed to non-statutory intangible embodiments. In view of Applicant's disclosure, paragraph 65 lines 10-12, the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., [ROM, RAM, magnetic disk storage media, optical storage media, flash memory devices]) and intangible embodiments (e.g., [electrical, optical, acoustical, carrier waves, infrared signals, digital signals]). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

3. Per claims 17 and 20, examiner suggests that applicant amend each claim to read as follows:
"An article of manufacture including a machine-accessible *tangible storage* medium...".

4. Per claims 18-19 and 21-24, examiner suggests that applicant amend each claims to read as follows:
"The article of manufacture of claim XX, wherein the machine-accessible *tangible storage* medium...".

The scope of claims 17-24 is understood by the examiner despite their rejection under statute 35 USC 101. They will be examined as though the above examiner suggestions have already been applied.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 4, 6-7, 12, 14-15, 20, and 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Yakovlev et al, U.S. Patent Application No. 10/449,276.

6. As per claim 1, Yakovlev discloses an apparatus, comprising:

- a standard hot-plug controller (paragraph 2 "hot-plug Peripheral Component Interconnect controllers (HPPC), figure 1 reference numeral 111), the standard hot-plug controller having a register (paragraph 24 "interface status registers", figure 1 reference numeral 109), for receiving at least one command from a microprocessor (paragraph 25, figure 1 reference numeral 102, 103, 105, 111), the standard hot-plug controller to:

- cause execution of a blinking pattern (paragraph 40, figure 4 reference numeral 408) on at least one light emitting diode (paragraph 32, figure 2 reference numeral 207 "power indicator", and 209 "attention indicator") associated with at least one target peripheral card interconnect slot (paragraph 32, figure 2 reference numeral 220 "PCI expansion slot) on a peripheral card interconnect bus (paragraph 28, figure 2 reference numeral 135 "PCI buses"),
- the blinking pattern to indicate the command being processed (paragraph 33 lines 9-25, figure 2 reference numeral 207 and 209).

7. As per claim 2, Yakovlev discloses the apparatus of claim 1, wherein the command is to turn the light emitting diode "on," "off," or make the diode blink in a blinking pattern having a duty cycle of approximately fifty percent (paragraph 41, figure 4 reference numeral 417).

8. As per claims 4, Yakovlev discloses an apparatus, comprising:

- a standard hot-plug controller (paragraph 2 "hot-plug Peripheral Component Interconnect controllers (HPPC), figure 1 reference numeral 111), the standard hot-plug controller having a register (paragraph 24 "interface status registers", figure 1 reference numeral 109), for receiving at least one command from a microprocessor (paragraph 25, figure 1 reference numeral 102, 103, 105, 111), the standard hot-plug controller to:
- cause execution of a blinking pattern (paragraph 40, figure 4 reference numeral 408) on at least one light emitting diode (paragraph 32, figure 2 reference numeral 207 "power indicator", and 209 "attention indicator") associated with at least one target peripheral card interconnect slot (paragraph 32, figure 2 reference numeral 220 "PCI expansion slot) on a peripheral card interconnect bus (paragraph 28, figure 2 reference numeral 135 "PCI buses"),

- the blinking pattern to indicate an error being processed (paragraph 33 lines 9-25, figure 2 reference numeral 207 and 209).

9. As per claim 6, Yakovlev discloses the apparatus of claim 4, wherein the blinking pattern is to indicated a hard error or a soft error (paragraph 33 lines 9-25 "operational error", figure 2 reference numeral 207 and 209. Claim 6 stating both 'a hard error and a soft error' would encompass all types of errors).

10. As per claim 12, Yakovlev discloses a method, comprising:
- receiving at least one command at a standard hot-plug controller from a microprocessor (paragraph 25, figure 1 reference numeral 102, 103, 105, 111); and
- causing execution of a blinking pattern (paragraph 40, figure 4 reference numeral 408) on at least one light emitting diode (paragraph 32, figure 2 reference numeral 207 "power indicator", and 209 "attention indicator") associated with at least one target peripheral card interconnect slot (paragraph 32, figure 2 reference numeral 220 "PCI expansion slot) on a peripheral card interconnect bus (paragraph 28, figure 2 reference numeral 135 "PCI buses"),
- the blinking pattern indicating an error occurring during processing of the command (paragraph 33 lines 9-25, figure 2 reference numeral 207 and 209).

11. As per claim 14, Yakovlev discloses the method of claim 12, wherein the biking pattern is indicating a hard error or a soft error (paragraph 33 lines 9-25 "operational error", figure 2 reference numeral 207 and 209. Claim 6 stating both 'a hard error and a soft error' would encompass all types of errors).

12. As per claim 20, Yakovlev discloses an article of manufacture including a machine-accessible *tangible storage* medium having data that, when accessed by a machine, cause the machine to perform the operations comprising (paragraphs 30-31):

- receiving a command at a standard hot-plug controller (paragraph 40, figure 4 reference numerals 406 and 408), from a microprocessor (paragraph 25, figure 1 reference numeral 102, 103, 105, 111); and
- cause execution of a blinking pattern (paragraph 40, figure 4 reference numeral 408) on at least one light emitting diode (paragraph 32, figure 2 reference numeral 207 "power indicator", and 209 "attention indicator") associated with at least one target peripheral card interconnect slot (paragraph 32, figure 2 reference numeral 220 "PCI expansion slot) on a peripheral card interconnect bus (paragraph 28, figure 2 reference numeral 135 "PCI buses"), and
- the blinking pattern indicating an error occurring during processing of the command (paragraph 33 lines 9-25, figure 2 reference numeral 207 and 209).

13. As per claims 7, 15, and 23, Yakovlev discloses a blinking pattern to indicate an error occurring after power is applied to the PCI slot (paragraph 33 lines 9-25, figure 2 reference numeral 207 and 209).

14. As per claim 24, Yakovlev discloses the article of manufacture of claim 20, wherein the machine-accessible *tangible storage* medium further includes data that cause the machine to perform operations comprising indicating a hard error or a soft error (paragraph 33 lines 9-25 "operational error", figure 2 reference numeral 207 and 209. Claim 6 stating both 'a hard error and a soft error' would encompass all types of errors).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

15. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yakovlev et al, U.S. Patent Application No. 10/449,276, in view of Tello, U.S. Patent No. 6463537.

16. Per claim 3, Yakovlev does not disclose: a command to enable or disable at least one target peripheral card interconnect slot.

- However, Tello discloses "The line PCI_CTRL 291 is used to disable or enable the PCI slot." (Tello, column 12, lines 22-23, figure 9 reference numeral 291).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Tello into the

system of Yakovlev to use a control line to enable or disable at least one target PCI slot. (Tello, column 12, lines 22-23, figure 9 reference numeral 291).

17. Claims 5, 13, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yakovlev et al, U.S. Patent Application No. 10/449,276.

18. Per claims 5, 13, and 21, Yakovlev does not disclose the blinking pattern indicating an error occurring before power is applied to the target slot. Yakovlev does disclose the indicator being illuminated to notify of an operator of an operation problem (paragraph 33 lines 9-25, figure 2 reference numeral 207 and 209).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to use the illuminated indicator of Yakovlev to notify an operator of an operation problem before power is applied to a target slot, because it would provide the new hot-plug PCI card from damaging due to overshot current.

19. Claims 8-10, 16-18, 22, 25, 26, 28, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yakovlev et al, U.S. Patent Application No. 10/449,276, in view of Cormier et al, U.S. Patent No. 4423949.

20. Per claims 8, 16, and 22, Yakovlev does not disclose: the blinking pattern has a duty cycle that is less than or greater than approximately fifty percent.

- However, Cormier discloses "an approximately fifty percent duty cycle (that is, LED 108 being on about one-half the time)", (column 4 lines 61-65, figure 2 reference numeral 108).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Cormier into the system of Yakovlev because one having ordinary skill in the art would want to have this convenient operating point for the duty cycle. (Column 4 lines 61-65, figure 2 reference numeral 108).

21. Per claims 9 and 17, Yakovlev discloses:

- receiving a command at a standard hot-plug controller (paragraph 40, figure 4 reference numerals 406 and 408), from a microprocessor (paragraph 25, figure 1 reference numeral 102, 103, 105, 111); and
- cause execution of a blinking pattern (paragraph 40, figure 4 reference numeral 408) on at least one light emitting diode (paragraph 32, figure 2 reference numeral 207 "power indicator", and 209 "attention indicator") associated with at least one target peripheral card interconnect slot (paragraph 32, figure 2 reference numeral 220 "PCI expansion slot) on a peripheral card interconnect bus (paragraph 28, figure 2 reference numeral 135 "PCI buses"),
- the blinking pattern to indicate the command being processed (paragraph 33 lines 9-25, figure 2 reference numeral 207 and 209),

Yakovlev does not disclose:

- the blinking pattern having a duty cycle that is less than or greater than approximately fifty percent.

However, Cormier discloses:

- the blinking pattern having a duty cycle that is less than or greater than approximately fifty percent (Cormier, column 4 lines 61-65, figure 2 reference numeral 108).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Cormier into the system of Yakovlev because one having ordinary skill in the art would want to have this convenient operating point for the duty cycle. (Column 4 lines 61-65, figure 2 reference numeral 108).

22. Per claims 10 and 18, Yakovlev discloses receiving a command to turn the light emitting diode "on," "off," or make the diode blink in a blinking pattern having a duty cycle of approximately fifty percent (paragraph 41, figure 4 reference numeral 417).

23. Per claims 25 and 28, Yakovlev discloses:

A system, comprising:

- a peripheral component interconnect bus (paragraph 28, figure 2 reference numeral 135 "PCI buses") having at least one peripheral component interconnect slot thereon (paragraph 32, figure 2 reference numeral 220 "PCI expansion slot), the peripheral component interconnect slot having at least one light emitting diode associated therewith (paragraph 32, figure 2 reference numeral 207 "power indicator", and 209 "attention indicator"),
- a bridge coupled to the peripheral component interconnect bus (paragraph 28, figure 2 reference numerals 108, 135, and 137), the bridge having a standard hot-plug controller coupled to the peripheral component interconnect bus (figure 2, reference numerals 111 and 137),

- the standard hot-plug controller to receive a command from a microprocessor (paragraph 25, figure 1 reference numeral 102, 103, 105, 111), and cause execution of a blinking pattern (paragraph 40, figure 4 reference numeral 408) on at least one light emitting diode (paragraph 32, figure 2 reference numeral 207 "power indicator", and 209 "attention indicator"),
- the blinking pattern to indicate the command being processed (paragraph 33 lines 9-25, figure 2 reference numeral 207 and 209), (from Claim 25)
- the blinking pattern to indicate an error occurring during processing of the command (paragraph 33 lines 9-25, figure 2 reference numeral 207 and 209), (from Claim 28)

Yakovlev does not disclose:

- the blinking pattern having a duty cycle that is less than or greater than approximately fifty percent (Cormier, column 4 lines 61-65, figure 2 reference numeral 108).

- However, Cormier discloses: the blinking pattern having a duty cycle that is less than or greater than approximately fifty percent (Cormier, column 4 lines 61-65, figure 2 reference numeral 108)

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Cormier into the system of Yakovlev because one having ordinary skill in the art would want to have this convenient operating point for the duty cycle. (Column 4 lines 61-65, figure 2 reference numeral 108).

24. Per claims 26 and 29, Yakovlev discloses the system further comprising a memory coupled to the bridge (Rohr, paragraph 25 "The MCH 105 also provides

an interface for communicating with a main memory 104." Figure 1 reference numerals 108 and 104).

25. Claims 11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yakovlev et al, U.S. Patent Application No. 10/449,276, in view of Cormier et al, U.S. Patent No. 4423949, further in view of Tello, U.S. Patent No. 6463537.

26. Per claims 11 and 19, Yakovlev and Cormier do not disclose: the command to enable or disable at least one target peripheral card interconnect slot.

- However, Tello discloses "The line PCI_CTRL 291 is used to disable or enable the PCI slot." (Tello, column 12, lines 22-23, figure 9 reference numeral 291).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Tello into the system of Yakovlev and Cormier because one having ordinary skill in the art would want to use this control line feature due to its' efficiency in allowing you to both enable and disable a PCI slot with only one control line (Tello, column 12, lines 22-23, figure 9 reference numeral 291).

27. Claims 27 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yakovlev et al, U.S. Patent Application No. 10/449,276, in view of Cormier et al, U.S. Patent No. 4423949, further in view of Cheung et al, U.S. Patent No. 6564329.

28. Per claims 27 and 30, Yakovlev and Cormier do not disclose: the system wherein the memory is a static random access memory (SRAM)

- However, Cheung discloses the system wherein the memory is a static random access memory (SRAM), (Cheung, column 5 lines 13-20, figure 2 reference numerals 214 and 218).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Cheung into the system of Yakovlev and Cormier because one having ordinary skill in the art would want benefit from the higher performance of a SRAM memory (Cheung, column 5 lines 13-20, figure 2 reference numerals 214 and 218).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Misiura whose telephone number is (571) 272-0889. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BTM

TIM VO
PRIMARY EXAMINER